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A

NEW UTILITY PATENT APPLICATION TRANSMITTAL

(to be used for new applications only)

Attorney Docket Number	9806
First Named Inventor	Jacob Jorné
Total Pages in this Submission	19

jc544 U.S. PTO
10/19/98

APPLICATION ELEMENTS

Notice: Checklist items mentioned under Application Elements section construct a new utility patent application. Please refer to MPEP Sections 506, 601, (37CFR 1.77, 1.53, 35 USC 111, 112, 113) for detailed explanation regarding completeness of an original patent application.

1. [√] Fee Transmittal Form (prescribed filing fee(s))
2. Specification
   - [√] Title of the Invention
   - [√] Cross References to Related Applications *(if applicable)*
   - [ ] Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   - [ ] Reference to Microfiche Appendix *(if applicable)*
   - [√] Background of the Invention
   - [√] Brief Summary of the Invention
   - [√] Brief Description of the Drawings *(if drawings filed)*
   - [√] Detailed Description
   - [√] Claim or Claims
   - [√] Abstract of the Disclosure
3. [√] Drawing(s) *(when necessary as prescribed by 35 USC 113)*
4. [√] Executed Declaration
5. Genetic Sequence Submission *(if applicable, all must be included)*
   - [ ] Paper Copy
   - [ ] Computer Readable Copy
   - [ ] Statement Verifying Identical Paper and Computer Readable Copy

ACCOMPANYING APPLICATION PARTS

jc525 U.S. PTO
09/174337
10/19/98

6. [ ] Assignment Papers
7. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
8. [ ] Computer Program in Microfiche
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Petition Checklist and Accompanying Petition
12. [ ] Preliminary Amendment
13. [ ] Proprietary Information
14. [ ] Return Receipt Postcard
15. [ ] Small Entity Statement
16. [ ] Additional Enclosures *(please identify below)*:

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Jacob Jorné
Signature	Jacob Jorné
Date	9-9-98

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Application Number			Class		Independent Claims	
Date of Receipt	Application Type		GAU		Total Claims	
	Filing Date		Foreign Filing License?		Drawing Sheets	
	Small Entity		Foreign Address?		Special Handling?	

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CUPRICON, Inc.

October 14, 1998

US Patent & Trademark Office
Washington, DC 20231

Dear Sir/Madam,

Enclosed please find the New Utility Patent Application 'Uniform Electroplating of Wafers", for your consideration.

Attached please find also a check of $395 to cover fee transmittal.

Sincerely,

Jacob Jorne

CUPRICON, Inc.
359 Westminster Road, Rochester, NY 14607
716-473-6322 (voice and fax)
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FEE TRANSMITTAL

Complete if Known	
Application Number	
Filing Date	9-9-98
First Named Inventor	Jacob Jorne
Group Art Unit	
Examiner Name	
Attorney Docket Number	9806

TOTAL AMOUNT OF PAYMENT ($)

METHOD OF PAYMENT (check one)

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number

Deposit Account Name

☐ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☐ Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance, 37 CFR 1.311(b)

2. ☐ Payment Enclosed:

☑ Check ☐ Money Order ☐ Other

FEE CALCULATION (fees effective 10/01/96)

1. FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	770	201	385	Utility filing fee	395.00
106	320	206	160	Design filing fee	
107	530	207	265	Plant filing fee	
108	770	208	385	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 395.00

2. CLAIMS

			Extra		Fee from below		Fee Paid
Total Claims	18	-20 =	0	X		=	
Independent Claims	2	-3 =	0	X		=	
Multiple Dependent Claims			0	X		=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim
109	80	209	40	Reissue independent claims over original patent
110	22	210	11	Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,460	147	2,460	For filing a request for reexamination	
112	900*	112	900*	Requesting publication of SIR prior to Examiner action	
113	1,790*	113	1,790*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	390	216	195	Extension for response within second month	
117	930	217	465	Extension for response within third month	
118	1,470	218	735	Extension for response within fourth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,470	138	1,470	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive unavoidably abandoned application	
141	1,290	241	645	Petition to revive unintentionally abandoned application	
142	1,290	242	645	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	650	244	325	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	230	126	230	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	770	246	385	Filing a submission after final rejection (37 CFR 1.129(a))	
149	770	249	385	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) ______

Other fee (specify) ______

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)

SUBMITTED BY

				Complete (if applicable)	
Typed or Printed Name	Jacob Jorné			Reg. Number	
Signature	Jacob Jorné	Date	9-9-98	Deposit Account User ID	

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United State Patent Application

Inventors: **Jacob Jorne; Judith A. Love**; both of Rochester, New York; both US citizens
Residence: 359 Westminster road, Rochester, NY 14607.
Assignee: **Cupricon, Inc.**, 359 Westminster Rd., Rochester, New York 14607

Title of the Invention:

UNIFORM ELECTROPLATING OF WAFERS

Related U.S. Application Data:

References Cited

U.S. Patent Documents

5,230,743	7/1993	Thompson et al.
5,429,733	7/1995	Ishida
5,445,172	8/1995	Thompson et al.

Other Publications

J. Jorne, Current Distribution of Copper Electroplating on wafers, Report, Cupricon, Inc., Rochester, NY (July 24, 1997).
H. S. Rathore and D. Nguyen, Copper Metallization for Sub-Micron Technology, in Advance Metallization Processes, VLSI Multilevel Interconnection, Santa Clara, CA, June 9, 1997.
P. Singer, Making the Move to Dual Damascene Processing, Semiconductor International, p. 79-82, August 1997.
P. Singer, Copper Goes Mainstream: Low k to Follow. Semiconductor International, pp. 67-70, November 1997.
C. H. Ting, V. M. Dubin and R. Cheung, Electrochemical Deposition of Copper for ULSI Metallization, paper 3.A,VLSI Multilevel Inteconnection Conference (1997).
M. Witty, S. P. Muraka and D. B. Fraser, SRC Workshop on Copper Interconnect Technology, Semiconductor Research Corporation, Research Triangle Park, NC (1993).
VLSI Multilevel Inteconnection Conference, VMCI, Santa Clara, CA (1997).

Attorney, Agent, or Firm-**Jorne & Love**, 359 Westminster Road, Rochester, NY 14607.

Summary of the Invention

The non-uniformity of electroplating on wafers is due to the appreciable resistance of the thin seed layer and edge effects. Mathematical analysis of the current distribution during wafer electroplating reveals that the ratio between the resistance of the thin deposited seed layer and the resistance of the electrolyte and the electrochemical reaction determines the uniformity of the electroplated layer. Uniform plating is critical in wafer

metallization for the subsequent step of chemical mechanical polishing of the wafer. Based on the analysis, methods to improve the uniformity of metal electroplating over the entire wafer include increasing the resistance of the electrolyte, increasing the distance between the wafer and the anode, increasing the thickness of the seed layer, increasing the ionic resistance of a porous separator placed between the wafer and the anode, establishing contacts at the center of the wafer, and jet electroplating by placement of a rotating distributor in front of the wafer. The rotating distributor generates multiple jets hitting the surface of the wafer, thus ensuring conformal electroplating. The jets can be either submerged in the electrolyte or above the level of the electrolyte. The distribution of holes in the distributor determines the distribution of electroplated metal on the wafer. The shape and uniformity of the electroplated layer can also be determined by the shape and relative size of the counter-electrode (anode), by masking the edge of the wafer and by periodically reversing the plating current. The problem of uniformity is more severe as the diameter of the wafer becomes larger.

18 claims, 5 drawing sheets

BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates to a plating device for achieving uniform plating of a wafer.

2. Background:

Copper Interconnect Technology

One of the primary challenges in IC design and fabrication is overcoming signal propagation delays, which are caused by resistance and capacitance within devices and interconnects. In high-speed circuits, the RC time delay becomes important in the form of a need for high conductivity. The high speed, combined with smaller dimensions, has made interconnect technology the focal point of current research and development. There is no question that the need for low RC will requires the use of new materials of lower resistance, such as copper, and low dielectric, such as polymers.

Aluminum is the most commonly used metal for metallization, along with its alloys and various silicides. However, in order to increase the conductivity, copper is expected to replace aluminum in the sub-0.25 μm technology, which is expected to be introduced into manufacturing within the very near future. Multilevel interconnect (MLI) technology will be used and consequently the interconnect current densities will be doubled, while contacts and cross-sectional areas will be decreased. This will result in higher power dissipation, calling for the introduction of highly reliable copper interconnect technology.

Cooper appears to offer low RC performance and high reliability over the commonly used aluminum alloys. The current approaches to copper metallization include CVD (blanket and selective), selective electroless deposition, sputtering (PVD) and electrodeposition. The common approaches to copper patterning include CMP, RIE and selective deposition. Copper CVD is based on two precursor chemistries, commonly used for Cu(I) and Cu(II) (see Witty et al., 1993). The growth rate is about 50nm/min and the resistivity is 2 mΩ-cm. Selective CVD of copper is preferred because fewer steps are needed, it is less expensive and smaller contacts and via can be filled. Many new and highly volatile Cu precursors have been developed, ranging from volatile solid Cu(I) coordination compounds to volatile liquid Cu(I) organometallics, which are capable of fast deposition of high purity Cu films at moderate temperatures. However, the various CVD processes for copper are expensive and relatively slow. It appears that electrochemical deposition of copper is the leading technology, as it offers low cost and fast deposition process. The main problems facing the commercialization of copper interconnect electrodeposition are the non-uniformity of the Cu layer over the wafer and the filling of small, high aspect ratio contact holes without void formation.

Because copper reacts with SiO_2, it is necessary to form a barrier layer first. Tantalum (Ta) or tantalum nitride (TaN) are pre-deposited on the SiO_2 by sputtering. Cu seed layer is needed next for good electrical contact and adhesion, thus thin Cu seed layer (500-1000A) is formed by sputtering or by CVD. In order to avoid any contact between the devices and copper, the first contact holes are filled with tungsten (W) sputtering. Copper electroplating is obtained from an aqueous solution of $CuSO_4$ and H_2SO_4, in the presence

of several additives and leveling agents. The electroplating is performed while the wafer is rotating at a speed of up to 2,000 rpm, while the electrolyte is pumped against the wafer in the form of a stagnation flow. Electrical contacts are established by hooks or a contact ring attached to the periphery of the wafer. This creates non-uniform current distribution due to the non-uniformity of the rotating disk geometry and due to the low resistivity of the thin copper layer (terminal effect). Using 8" wafer, the non-uniformity of the layer thickness reaches 9-15% 1σ, as the thickness at the edge is 13-15KA, while in the center the thickness is 7.5-10 KA. This results in loosing as much as 1.5" of edge during polishing, as the edge remains Cu-covered while the center area is completely polished. Commercial electroplating units include Equinox and LT-210 made by Semitool, Montana (U.S. patents 5,230,743 and 5,445,172), in which the wafer is held by flexibly mounted gripping fingers. Another source is EEJA (Electroplating Engineers of Japan), where the contact hooks are replaced by a contact ring and air bag (U.S. patent 5,429,733). All these electroplating systems suffer from non-uniform distribution of plating, resulting in excess of electroplated metal at the circumference edge of the wafer. Literature on copper technology is available at VMIC conference proceedings (Rathore & Nguyen 1997, Ting 1997, VMIC 1997).

Copper interconnect technology requires the use of damascene processing because etching of copper is extremely difficult. Damascene processing involves the formation of interconnect lines by first etching trenches in a planar dielectric layer, and then filling these trenches with the metal, such as aluminum or copper (Singer 1997). After filling, the metal and the dielectric are planarized by chemical-mechanical polishing (CPA). In dual damascene processing, a second level is involved where series of holes (contacts or via) are etched and filled in addition to the trenches. Dual damascene will mostly be the patterning choice for copper interconnects (Singer 1997).

Current Distribution of Metal Electroplating on Wafers

The current distribution for metal electroplating on wafers has been analyzed (see Jorne 1997). The non-uniformity of the plating is due to the appreciable resistance of the thin

seed layer and the geometry of the electroplating system. When the current is fed from the circumference edge of the wafer, a non-uniform plating occurs as thicker metal deposit occurs at the edges. The ratio between the resistance of the thin metal layer and the resistance of the electrolyte and the electrochemical reaction determines the uniformity of the electroplating. Increasing the diameter of the wafer and the resistivity of the seed layer results in non-uniformity, while increasing the resistivity of the electrolyte and the electrochemical reaction results in higher uniformity.

A mathematical analysis of the plating current distribution over the wafer (Jorne 1997) shows that the electroplating current density is given by

$$i_z/i_{avg} = (B/2)I_0(Bx)/I_1(B)$$

where i_z and i_{avg} are the local and average current densities, respectively. I_0 and I_1 are the modified Bessel functions of order 0 and 1, respectively. $x=r/R$ is the ratio of the local radius r to the outer radius of the wafer R, and B is the plating uniformity parameter defined by

$$B^2 = (\rho/\rho_{el})(R^2/Wd)$$

where ρ and ρ_{el} are the resistivities of the electroplated metal and the electrolyte, respectively, R is the radius of the wafer, W is the thickness of the seed layer and d is the distance between the wafer and the counter electrode. In order to ensure uniformity during electroplating, the electroplating system must obey that the value of B is smaller than unity: $B^2 \leq 1$. The current distribution, and hence the thickness distribution of the electroplated metal depends on a single parameter B, which represents the ratio between the resistance of the deposit and the electrochemical resistance of the electrolyte and the electrochemical reaction. For small B ($B^2 \leq 1$), the plating distribution is fairly uniform, however, for large B ($B^2 \geq 1$), the plating distribution becomes progressively non-uniform as the deposit at the circumference becomes thicker.

SUMMARY OF THE INVENTION

The present invention describes several electroplating devices for the uniform metallization of wafers for interconnect technology. The invention addresses in particular the problem of achieving uniform plating distribution over the entire wafer and the conformity to sub-micron features. The wafer, on which a thin barrier layer and seed layer are pre-deposited, is brought in contact with an electrolytic solution made of a salt of the metal to be deposited, supporting electrolytes and leveling agents. Because the seed layer is very thin, the electroplating rate becomes lower at further distances from the contact point, as the electrical current has to flow through the high-resistance thin seed layer. In conventional wafer plating systems, the wafer is held at its edge by gripping fingers or a contact ring, through which the electrical current is fed. This usually results in higher plating at the circumference edge, creating severe problems during the subsequent chemical-mechanical polishing step. In the present invention, the current distribution during wafer electroplating is mathematically analyzed. The uniformity of electroplating depends on the ratio of the resistance of the seed layer to the resistance of the electrolyte and the electrochemical reaction. Uniformity of electroplating can be achieved by maintaining the uniformity parameter B below a certain value, usually below unity. This can be achieved by decreasing the seed layer resistance, increasing the electrolyte resistance, increasing the distance between the wafer and the counter electrode, by a jet electroplating using a rotating distributor, and by increasing the electrical resistance of a porous separator which is placed between the wafer and the counter electrode. Jet electroplating can be achieved by pumping the electrolyte trough a rotating distributor with small holes (rotating shower head). The resulting multiple jets hit the surface of the wafer thus ensuring uniform and conformal electroplating, in the presence or in the absence of leveling agents and brightening additives. Predetermined distribution of electroplating can be achieved by nonuniform distribution of holes in the distributor. The more holes per unit area results in heavier electrodeposit on the corresponding area of the wafer facing the distributor. Furthermore, the uniformity of the electroplated layer can be determined by the shape and size of the counter electrode and its position relative to the wafer. Uniformity can be achieved also by periodically reversing the current during plating, thus preferentially dissolving the excess metal from

areas where the electroplating was higher. In addition, instead of the wafer being electrically connected by contact grips at the edge, the wafer could rest on vertical contact pegs placed in the electrolyte and electrically isolated from the electrolyte. Only the tips of these pegs touch the active side of the wafer to be plated. The wafer, resting on contact pegs or a contact ring, is rotating, while the electrolyte solution is being upwardly pumped against the wafer in order to achieve uniform concentration in the electrolyte, good conformity and uniform plating distribution. The electrical contact points can be also distributed over the entire surface of the wafer, preferentially at the center, thus eliminating thicker electroplating at the edges and ensuring uniformity over the entire wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic view of an electroplating apparatus, showing the contact fingers or ring and the wafer being rotating while the electrolytic solution is circulated against the wafer. The edge of the wafer is shielded from being heavily plated by an insulating ring.

Fig. 2 shows an electroplating apparatus, in which the wafer is resting on several contact pegs vertically located in the electrolyte. The electrical current is distributed over the entire wafer, thus eliminating plating non-uniformity.

Fig. 3 is a schematic view of submerged jet electroplating apparatus showing a stationary wafer, while the electrolyte is circulated against the wafer through a circular distributor, in which many holes are drilled in an angle in such a way that the circulating electrolyte causes the distributor to rotate. The electrolyte is emerging from the holes as submerged jets, thus improving the conformity and uniformity of the deposit.

Fig. 4 is a schematic view of jet electroplating apparatus in which the electrolyte level is maintained below the wafer, and where the electrolyte is pumped through a rotating distributor and forms multiple jets hitting the wafer. The wafer is not submerged in the electrolyte and only the multiple jets serve as electrolyte paths for the current.

Figure 5 shows a schematics of the rotating distributor. The electrolyte is pumped through the holes of the distributor and emerges as multiple jet hitting the wafer. Some of the holes are drilled in an angle, causing the distributor to rotate.

DESCRIPTION OF PREFERRED EMBODIMENT

The preferred embodiments will be discussed hereinafter with reference to the drawings. The wafer **1** is obtained by lithographic etching and deposition processes, commonly used in the microelectronics industry. The sub-micron width or diameter of the trenches and via holes are, as a typical example, about 0.25 micron, with a high aspect ratio, typically as an example, of about 1:4. Thus the depth of the trenches or holes could be about 1 micron or more. The barrier layer typically consists of Ta or TaN or other metals or compounds capable of preventing the diffusion and reaction of the intended interconnect metal, say copper for example, with the dielectric, say SiO_2 for example. The barrier layer is usually obtained by CVD, PVD or sputtering. Seed layer of the metal **10**, say copper for example, is deposited on the barrier layer in order to act as the conducting electrode for the subsequent electroplating of the metal. The seed layer is obtained by CVD, PVD or sputtering to a typical thickness of about 0.1 micron. The seed layer is fully conformed to the walls of the patterned trenches and holes and via.

The wafer **1** is then transferred to the electroplating apparatus **7** as it is facing down gripped by the contacts **9**, as shown in Fig. 1. The contacts **9**, as shown in Fig. 1, consist of metallic conductor **3**, electrically insulated from the electrolytic solution by a plastic insulator **14**, except at the tips which are in direct contact with the electroplated metal **10** on the wafer **1**. The rotation is designed to ensure uniformity of the plating and averaging possible disturbances. The electrolyte **6** is pumped upwardly against the surface of the wafer to ensure sufficient supply of reacting ions to the surface and into the sub-micron trenches and holes and exits by flowing over the overflow **16** which determines the level of the electrolyte in the apparatus **7**. The electrolyte is circulated from outer reservoir **25** by pump **26** into the inner reservoir **27**. A porous separator **8** is located between the anode **2** and the wafer **1** to ensure even distribution of the flow **6** over the entire wafer **1**. The porosity and thickness of the porous separator **8** also determines the electrical resistance of the electrolyte and the uniformity of the electroplating **10** on the wafer **1**. A masking ring **12** is placed at a certain distance from the wafer to shield the edge of the wafer from heavy electroplating there. The anode **2**, made of the plated metal, is located below the wafer and is usually smaller in diameter than the wafer itself. The circumference edge of the wafer is masked by a plastic ring **5** which masks the edge by

forming a less than 90 degree angle of contact, as shown in Fig. 1. The wafer is resting on the ring **5** and the contacts in such a way that its backside is not submerged in the electrolyte and only the active side of the wafer is in contact with the fountain of electrolyte **6** formed by pumping the electrolyte against the wafer **1**.

Fig. 2 shows a design of an electroplating device where the electrical current is distributed through several contact points **9**, thus eliminating the non-uniformity in electroplating. The wafer **1** is resting, facing downward, against several pegs **14** vertically positioned inside the electrolyte. The tips **9** of these pegs **14** are in electrical contact with the active face of the wafer where electroplating is taking place **10**. The electrical wires **15** are insulated from the electrolyte by the insulating pegs. The wafer **1** is resting also on an insulating ring **5,** which masks the edge of the wafer **1** from developing thick deposit. The entire contact pegs assembly **14** and the insulating ring **5** and the wafer **1** are rotating while electrolyte **6** is pumped upwardly against the surface of the wafer to ensure uniformity and conformity to the high aspect ratio trenches and holes, previously etched in the wafer. A masking ring is placed at a certain distance from the wafer to shield the edge of the wafer from heavy electroplating there. A porous separator **8** is located between the anode **2** and the wafer **1** to ensure even distribution of the flow **6** over the entire wafer **1**. The porosity and thickness of the porous separator **8** also determines the electrical resistance of the electrolyte and the uniformity of the electroplating **10** on the wafer **1**. The electrolyte is circulated by a pump **26** from the outer reservoir **25**, through the feeding pipe **28** into the inner reservoir **27**.

Fig. 3 shows a design of electroplating apparatus where the wafer is stationary and a rotating distributor **21** is placed in close proximity to the wafer. The distributor **21** is made of a plastic disk with many holes **22,** some are drilled in an angle to the direction of the flow of the electrolyte. The electrolyte is pumped through these holes, causing the distributor to rotate, sending multiple jets of electrolyte **23** impinging on the stationary or rotating wafer **1**. The distribution of holes on the rotting distributor determines the local distribution of electroplating on the wafer. The more holes per unit are results in thicker electroplating there. It is possible to set the distribution of electroplating by the density of holes in various radial positions on the distributor. The rotating distributor is resting on a pin **24**, centrally located on top of the feed pipe **28**. The electrolyte is pumped from the

outer reservoir **25** by a pump **26** and into the inner reservoir **27**, through an inlet **28** located below the anode **2**. The electrolyte passes around the anode **2** and through the porous separator **8**, and then upward through the rotating distributor **21** and emerges in the form of multiple jets **23** impinging on the wafer **1**. The electrolyte **6** then overflows over the smooth edge **16** of the inner reservoir **27** to the outer reservoir **25**. A plastic ring **5** shields the edge of the wafer from heavy electroplating there. The electrical contacts **9** are made from the metal being deposited (e.g. copper) and are not insulated, thus serving as current thieves, preventing heavy deposit at the contact points. The inner reservoir **11** is placed inside the outer reservoir **7** and resting on several legs **29**. A porous separator **8** is placed between the anode **2** and the rotating distributor **21** in order to increase the electrical resistivity of the electrolyte **6**. The wafer **1** is resting on several electrical contacts **9** and the current is fed by wires **3**. The wafer **1** is pressed against the contacts **9** by the cover of the reservoir **30**.

Fig. 4 shows a design of an electroplating apparatus in which the wafer is stationary and the level of the electrolyte is maintained below the face of the wafer. The electrolyte is pumped by a pump **26**, through the inlet **28** into the inner reservoir **27**, where it flows around the anode **2** and up against the rotating distributor **21**. The distributor is made of a plastic disk through which many holes **22** are drilled, some in an angle to the direction of the flow. This allows the distributor **21** to rotate, while the electrolyte emerges in the form of multiple jets, hitting the face of the stationary or rotating wafer **1**. The distributor rests on a pin **24**, centrally located on top of the inlet pipe **28**. The electrolyte overflows over the smooth edge **16** of the wall **11** of the inner reservoir **27** into the outer reservoir **25**. The inner reservoir **11** is placed inside the outer reservoir **7** and stands on several legs **29**. The distance between the rotating distributor and the wafer is small to allow an effective impinging flow which is necessary to achieve conformity and uniformity during the electroplating of the wafer. The overflow maintains that the level of the electrolyte in the inner reservoir **27** is slightly above the rotating distributor **21**.

Fig. 5 shows the rotating distributor **21**. It consists of plastic disk through which multiple holes **22** are drilled. Some of the holes are drilled in an angle to the flow direction, thus causing the distributor **21** to rotate around its axis **24**. The electrolyte emerges from the holes as multiple jets, hitting the surface of the wafer, where electroplating takes place.

We claim:

1. An electroplating device for the metallization of wafers for interconnection. The wafer, previously coated with a thin barrier layer and a thin seed layer of the electroplated metal, is placed and pressed against contact fingers or a ring and rested on an insulating ring which masks the circumference edge of the wafer. The wafer is rotated or is held stationary with respect to the plating bath. The electrolyte is pumped upward against the wafer. A plating uniformity parameter is defined:

$$B^2 = (\rho/\rho_{el})(R^2/Wd)$$

where ρ and ρ_{el} are the resistivities of the electroplated metal and the electrolyte, respectively, R is the radius of the wafer, W is the thickness of the electroplated metal and d is the distance between the wafer and the counter electrode. In order to ensure uniformity during electroplating, the electroplating system must obey that the value of B^2 is smaller than unity: $B^2 \leq 1$. This implies that the geometry of the electroplating device is such that the square of the wafer radius divided by the product of the width of the seed layer and the distance between the wafer and the counter electrode must be smaller than the ratio of the resistivities of the electrolyte and the electroplated metal:

$$R^2 / Wd \leq \rho_{el} / \rho$$

2. An electroplating device for wafer metallization as set forth in claim 1, wherein the resistance of the electrolyte is increased by placing a non-conducting porous separator, a distributor or a porous membrane between the wafer and the counter electrode, thus increasing the ionic resistance of the electrolyte and ensuring uniform electroplating.

3. An electroplating device for wafer metallization as set forth in claim 1, wherein the electrochemical resistance is increased by adding leveling agents to the electrolyte which tend to adsorb at the electroplated metal, thus increasing the charge transfer resistance at the metal/electrolyte interface and ensuring uniform and conformal electroplating.

4. An electroplating device for wafer metallization as set forth in claim 1, wherein the distance between the wafer and the counter electrode d is increased in order to reduce the value of the uniformity parameter B, thus ensuring uniform electroplating.

5. An electroplating device for wafer metallization as set forth in claim 1, wherein the thickness of the seed layer W is increased in order to decrease the uniformity parameter B and to ensure uniform electroplating over the entire wafer.

6. An electroplating device for wafer metallization as set forth in claims 1, wherein the diameter of the counter electrode is smaller than the diameter of the wafer.

7. An electroplating device for wafer metallization as set forth in claims 1 wherein a rotating distributor is placed in front of the wafer. The distributor is rotating by the flow of electrolyte through some of the holes that are drilled in an angle to the flow direction. The electrolyte emerges from the distributor in the form of multiple submerged jets hitting the face of the wafer, thus ensuring uniformity and conformity, in the presence or even in the absence of electroplating additives such as leveling agents and brighteners. Uniform or predetermined nonuniform distribution of electroplating can be achieved by uniform or nonuniform distribution of holes in the distributor, respectively.

8. An electroplating device for wafer metallization as set forth in claims 1 wherein a rotating distributor is placed in front of the wafer. The distributor is rotating by the flow of electrolyte through some of the holes that are drilled in an angle to the flow direction. The level of the electrolyte is maintained below the face of the wafer and slightly above the rotating distributor. The electrolyte emerges from the distributor in the form of multiple jets hitting the surface of the wafer. The jets also serve as the ionic path for the passage of current between the anode and the cathode. The jets ensure the uniformity and conformity of the electroplating process, in the presence or even in the absence of electroplating additives such as leveling agents and brighteners. Uniform or predetermined nonuniform distribution of electroplating can be achieved by uniform or nonuniform distribution of holes in the distributor, repectively.

9. An electroplating device for wafer metallization as set forth in claims 1, wherein the current is periodically reversed in order to remove excess electroplated metal from areas on the wafer where the electroplating is thicker than the average. The total electrical charge passed during the reversed current period must be smaller than the total charge passed during the forward current period.

10. An electroplating device for wafer metallization as set forth in claim 1, wherein pulsed current is applied during the electroplating process in order to achieve uniformity and conformity to the high aspect ratio trenches, holes and via which are patterned on the surface of the wafer.

11. An electroplating device for wafer metallization as set forth in claim 1 wherein the wafer is stationary and the whole electroplating apparatus is rotating.

12. An electroplating device for the metallization of wafers for interconnection. The wafer, previously coated with a thin barrier layer and a thin seed layer of the electroplated metal, is placed and pressed against contact pegs and rested on an insulating ring which masks the circumference edge of the wafer. The electrically conducting peg are insulated from the electrolyte by insulating sleeves, except at the points of contact with the wafer. The electrolyte is pumped upward against the wafer. One or multiple contact pegs are spatially distributed over the surface of the wafer in order to ensure uniform electroplating of the metal over the entire wafer. Feeding the electrical current from a contact to the center of the wafer and from various contact points ensure uniformity in the thickness of the electroplated metal layer.

13. An electroplating device for wafer metallization as set forth in claim 12, wherein the contact pegs assembly and the wafer are rotating together in order to ensure uniform plating.

14. An electroplating device for wafer metallization as set forth in claim 12, wherein the electrolyte is pumped upward against the wafer which is resting on the contact pegs and the insulating ring.

15. An electroplating device for wafer metallization as set forth in claim 12, wherein the contact pegs assembly and the wafer are rotating and the electrolyte is pumped upward against the rotating wafer, whose only active surface is exposed to the liquid while the back side is outside the electrolyte.

16. An electroplating device for wafer metallization as set forth in claims 12, wherein the current is periodically reversed in order to remove excess electroplated metal from areas on the wafer where the electroplating is thicker than the average. The total electrical charge passed during the reversed current period must be smaller than the total charge passed during the forward current period.

17. An electroplating device for wafer metallization as set forth in claim 12, wherein pulsed current is applied during the electroplating process in order to achieve uniformity and conformity to the high aspect ratio trenches, holes and via which are patterned on the surface of the wafer.

18. An electroplating device for wafer metallization as set forth in claim 12 wherein the wafer is stationary and the whole electroplating apparatus is rotating.

*   *   *   *   *

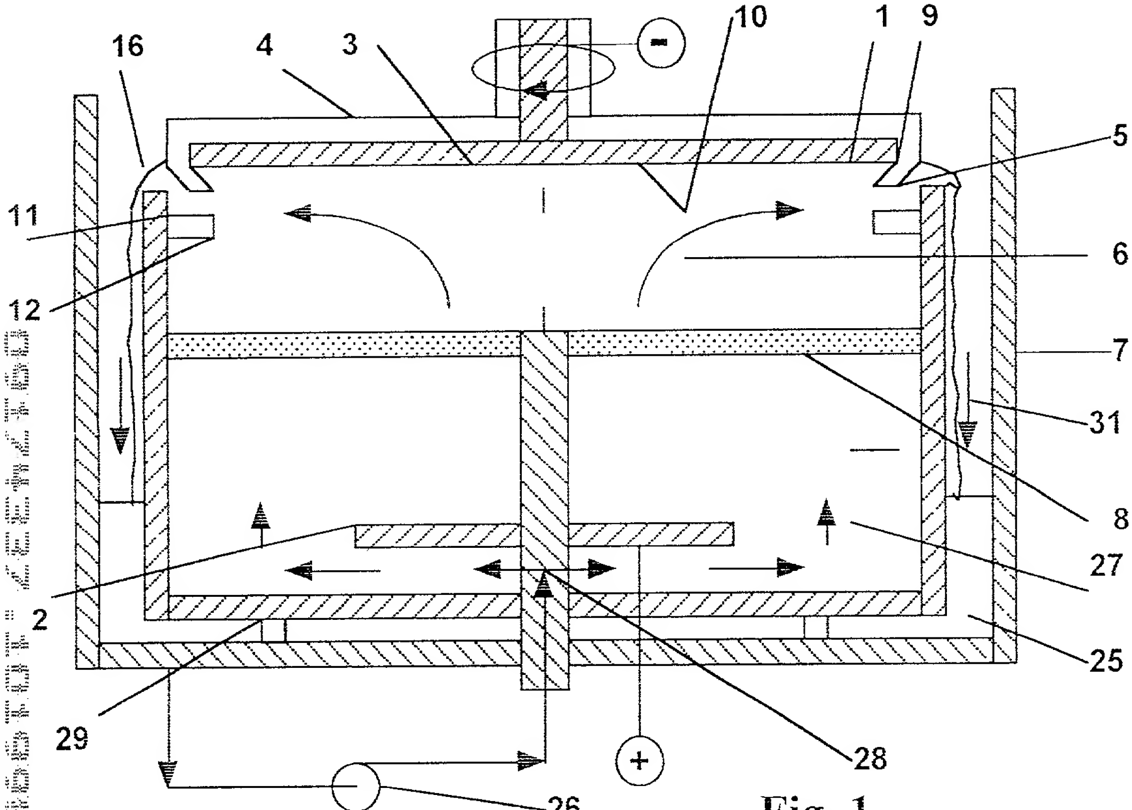

Fig. 1

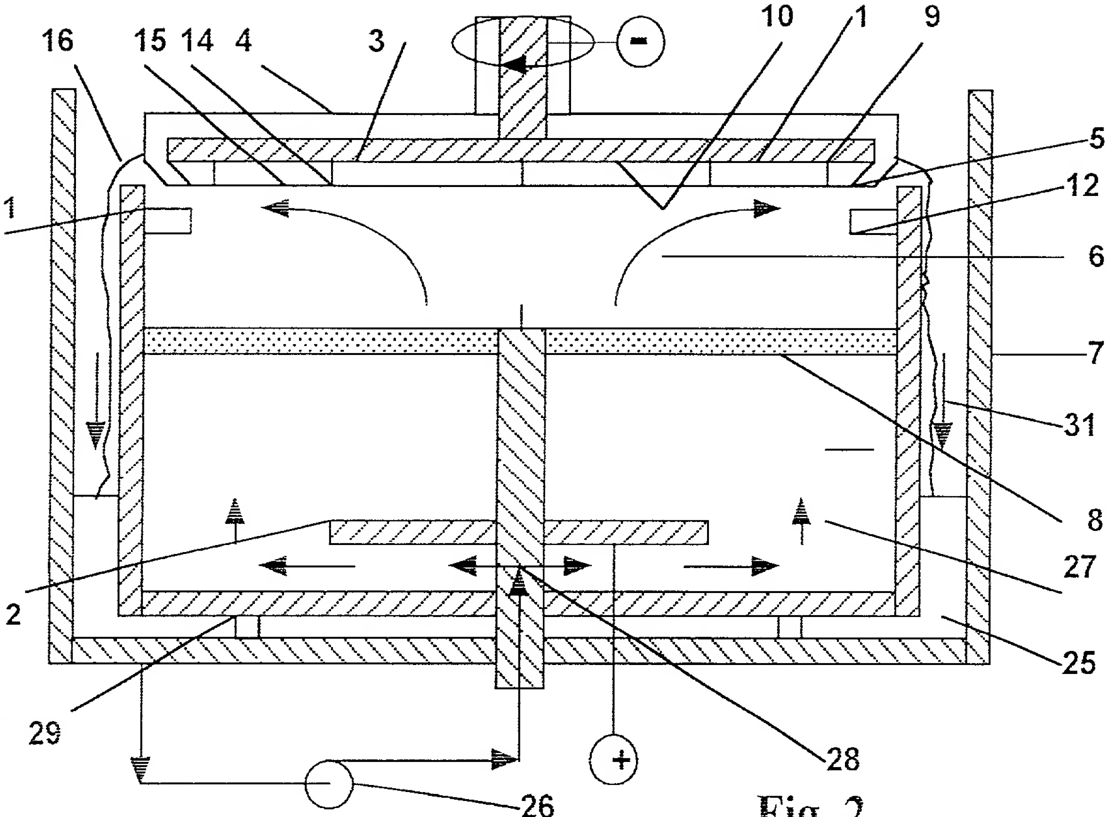

Fig. 2

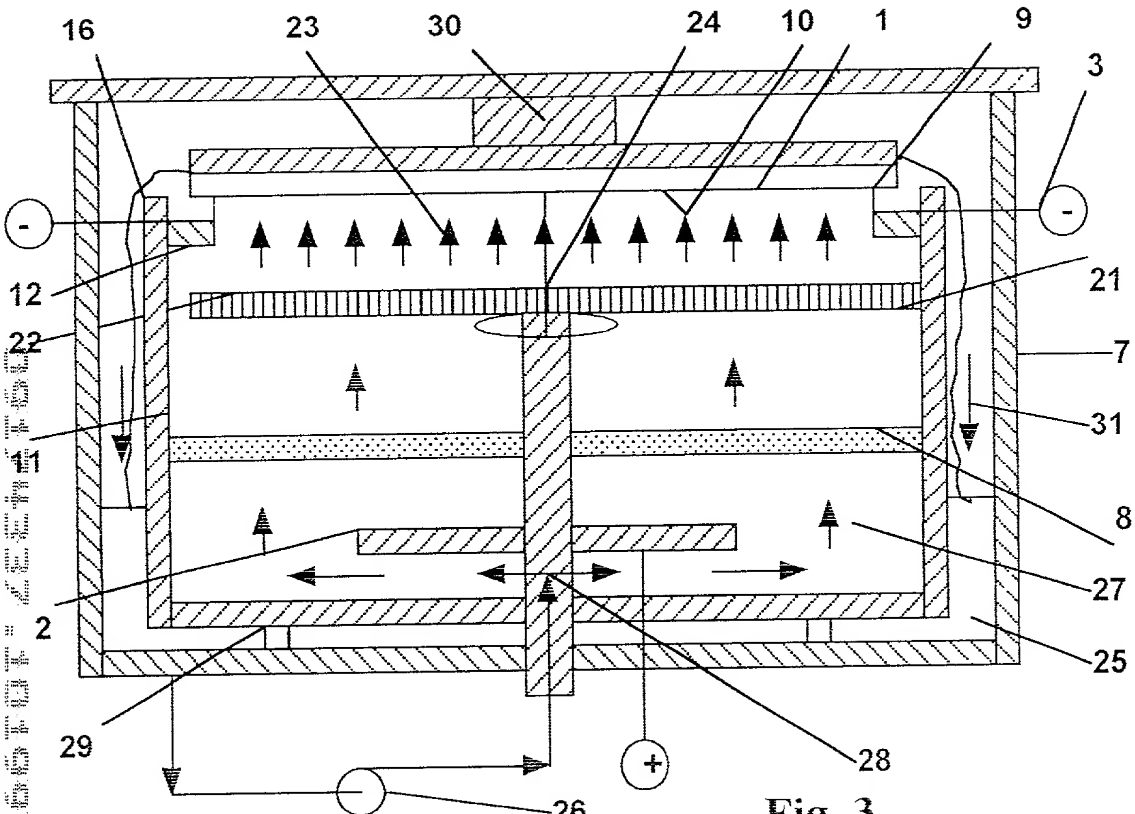

Fig. 3

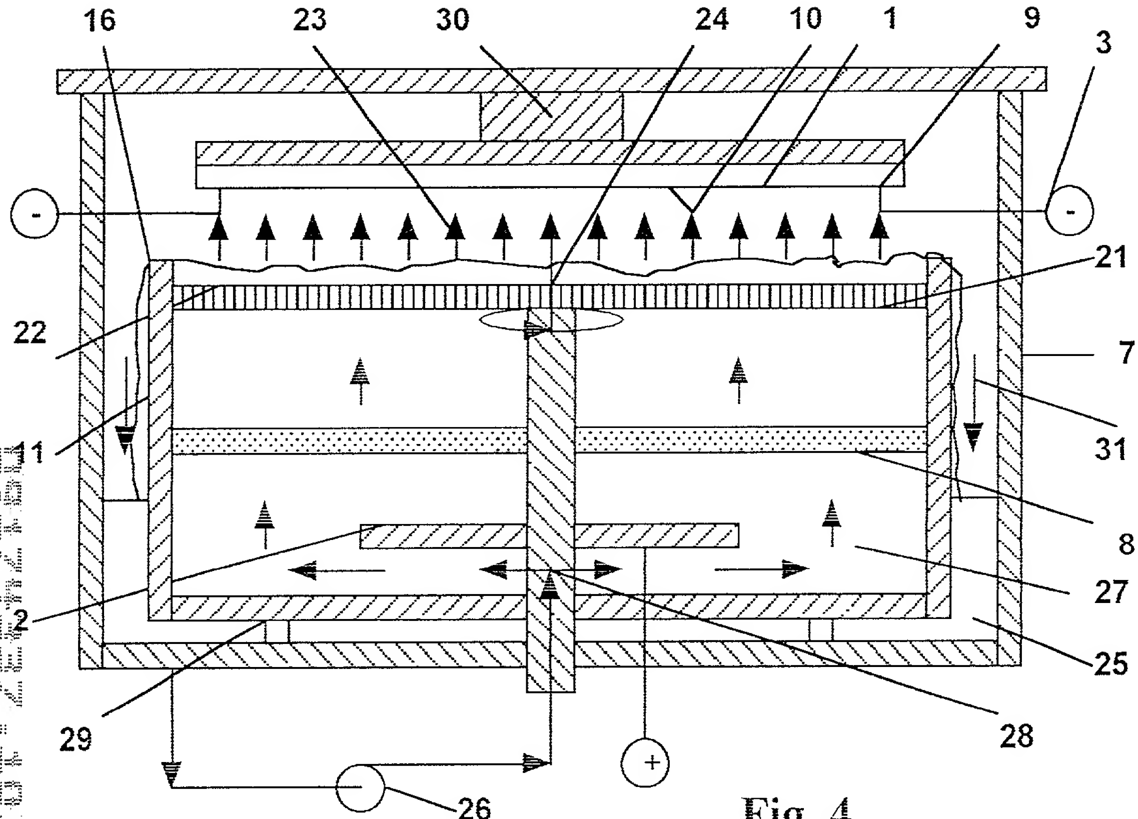

Fig. 4

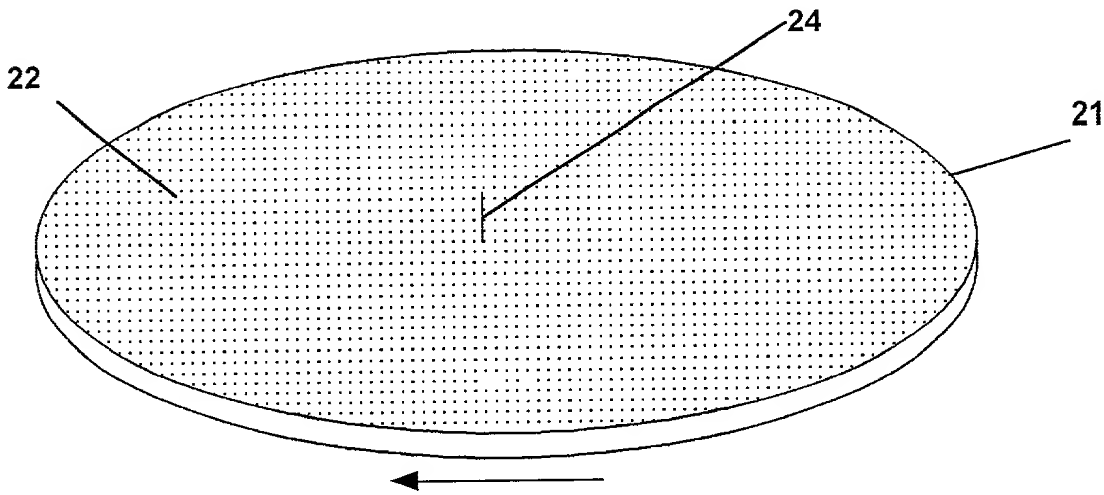

Fig. 5

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VERIFIED STATEMENT CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) & 1.27(c))–SMALL BUSINESS CONCERN

Docket Number (Optional) 9806

Applicant or Patentee: Jacob Jorné
Application or Patent No.: ______
Filed or Issued: ______
Title: Uniform Electroplating of Wafers

I hereby declare that I am
☒ the owner of the small business concern identified below:
☐ an official of the small business concern empowered to act on behalf of the concern identified below

NAME OF SMALL BUSINESS CONCERN Cupricon, Inc.
ADDRESS OF SMALL BUSINESS CONCERN 359 Westminster Road
Rochester, NY 14607

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time, or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention described in:

☐ the specification filed herewith with title as listed above.
☒ the application identified above.
☐ the patent identified above.

If the rights held by the above identified small business concern are not exclusive, each individual, concern, or organization having rights in the invention must file separate verified statements averring to their status as small entities, and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern, or organization having any rights in the invention is listed below:
☒ no such person, concern, or organization exists.
☐ each such person, concern, or organization is listed below

Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING JACOB JORNÉ
TITLE OF PERSON IF OTHER THAN OWNER ______
ADDRESS OF PERSON SIGNING 359 Westminster Rd. Rochester, NY 14607
SIGNATURE Jacob Jorné DATE 9-9-98

Burden Hour Statement. This form is estimated to take 0.3 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231

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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION

☑ Declaration Submitted with Initial Filing OR ☐ Declaration Submitted after Initial Filing

Attorney Docket Number	9806
First Named Inventor	Jacob Jorné
COMPLETE IF KNOWN	
Application Number	
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled :

Uniform Electroplating of Wafers

(Title of the invention)

the specification of which

☑ is attached hereto

OR

☐ was filed on (MM/DD/YYYY) ______ as United States Application Number or PCT International Application Number ______ and was amended on (MM/DD/YYYY) ______ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code §119 (a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or §365 (a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)

☐ Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

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DECLARATION — Utility or Design Patent Application

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s), or §365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application Number	PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: ☐ Customer Number [ ] → Place Customer Number Bar Code Label here
OR
☐ Registered practitioner(s) name/registration number listed below

Name	Registration Number	Name	Registration Number

☐ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto.

Direct all correspondence to: ☐ Customer Number or Bar Code Label [ ] OR ☐ Correspondence address below

Name					
Address					
Address					
City		State		ZIP	
Country		Telephone		Fax	

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])				Family Name or Surname			
Jacob —				Jorné			
Inventor's Signature	Jacob Jorné					Date	9-9-98
Residence: City	Rochester	State	NY	Country	USA	Citizenship	USA
Post Office Address	359 Westminster Road						
Post Office Address							
City	Rochester	State	NY	ZIP	14607	Country	USA

☑ Additional inventors are being named on the 1 supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto

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DECLARATION	ADDITIONAL INVENTOR(S) Supplemental Sheet Page ___ of ___

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])					Family Name or Surname		
Judith Ann					Love		
Inventor's Signature	Judith A. Love					Date	9-9-98
Residence: City	Rochester	State	NY	Country	USA	Citizenship	USA
Post Office Address	359 Westminster Road						
Post Office Address							
City	Rochester	State	NY	ZIP	14607	Country	USA

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])					Family Name or Surname		
Inventor's Signature						Date	
Residence: City		State		Country		Citizenship	
Post Office Address							
Post Office Address							
City		State		ZIP		Country	

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])					Family Name or Surname		
Inventor's Signature						Date	
Residence: City		State		Country		Citizenship	
Post Office Address							
Post Office Address							
City		State		ZIP		Country	

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DECLARATION — Supplemental Priority Data Sheet

Additional foreign applications:

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
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			☐	☐	☐

Additional provisional applications:

Application Number	Filing Date (MM/DD/YYYY)

Additional U.S. applications:

U.S. Parent Application Number	PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number *(if applicable)*

09/147337

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DECLARATION

REGISTERED PRACTITIONER INFORMATION (Supplemental Sheet)

Name	Registration Number	Name	Registration Number